

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes first and second CMOS (complementary metal oxide semiconductor) inverter circuits each having a latch structure and a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line. The device further includes a selection circuit to apply one of a first voltage and a second voltage different from the first voltage to a power supply node of at least the second CMOS inverter circuit. The selection circuit applies the second voltage to the power supply node of the second CMOS inverter circuit at least in "1" data write mode.